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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/592,572	DELLACONA, RICHARD	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's Response mailed on July 30, 2004. Claims 1-36 of the application are pending. This office action is made non-final.

Drawings

2. The drawings submitted on July 30, 2004 are accepted.

Specification

3. The disclosure is objected to because of the following informalities:

Page 3, Line 31, "In a one configuration with two or more computers" appears to be incorrect, and it appears that it should be "In one configuration with two or more computers".

Page 8, Lines 29-30, "Referring to Figure 2, the mass storage array 200 includes one or more modules 202A, 202B... 202n" appears to be incorrect, and it appears that it should be "Referring to Figure 3, the mass storage array 200 includes one or more modules 202A, 202B... 202n".

Appropriate corrections are requested.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-5, 7 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Keaveny et al.** (U.S. Patent 6,065,087), **Swanson et al.** (U.S. Patent 6,580,531) and **Dekoning et al.** (U.S. Patent 6,055,228).

6.1 **Leshem** teaches Data storage system. Specifically, as per Claim 1, **Leshem** teaches a high speed mass storage system (CL1, L4-8; CL1, L33-37; Abstract, L11-14); comprising at least one module containing:

at least one CPU (Fig 1, Item 22; CL3, L26-27);

a plurality of plug-in storage devices for storing information (Abstract, L1-3; Abstract, L11-17; Fig 1; Fig 2); and

a storage device bypass circuit board associated with each storage device each storage device being plugged into a connector on the storage device bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation. **Espy** teaches that high speed mass storage system which is readily expandable to increase its storage capacity while the system is in operation (Page 1, L19-24), as that will enable to add an additional disk array chassis to the existing system when additional memory space is required, without shutting down the existing system (Page 1, L19-24). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included high speed mass storage system which would be readily expandable to increase its storage capacity while the system was in operation. The artisan would have been motivated because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system.

Leshem teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach a module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. **Keaveny et al.** teaches a circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included a circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

Leshem teaches a controller providing a communication path between the CPU with some of the storage devices through its associated storage device bypass circuit board (CL3, L33-36; CL3, L40-50). **Leshem** does not expressly teach a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board and through the module bypass circuit board. **Dekoning et al.** teaches a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board (Fig 7; CL3, L36-41), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board. The artisan would have been motivated because that would enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

Leshem does not expressly teach a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board and through the module bypass circuit board through the module bypass circuit board. **Espy** teaches a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board and through the module bypass circuit board (Page 2, L5-23; Fig 1, Item 40; Page 6, L7-16), as that will enable to add an additional disk array chassis to the existing system when additional memory space is

required, without shutting down the existing system (Page 1, L19-24). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included a controller providing a communication path between the CPU with each of the storage devices through its associated storage device bypass circuit board and through the module bypass circuit board. The artisan would have been motivated because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system.

6.2 As per Claim 2, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem** does not expressly teach that each storage device bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present. **Dekoning et al.** teaches that each storage device bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present (Fig 6; CL11, L30-60), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included each storage device bypass circuit board including a circuit which completed the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device was present. The artisan would have been motivated because that would enable

detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

6.3 As per Claim 3, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that the module bypass circuit board outputs electrical signals from the at least one module via the optical input/output connector when light signals are received by the optical input/output connector. **Keaveny et al.** teaches a circuit board that outputs electrical signals from the at least one module via the optical input/output connector when light signals are received by the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that outputted electrical signals from the at least one module via the optical input/output connector when light signals were received by the optical input/output connector. The artisan would have been motivated

because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

6.4 As per Claim 4, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach first and second modules each including elements (a) through (e) as discussed in Paragraph 7.1 above. **Leshem** does not expressly teach that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light. **Keaveny et al.** teaches that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** with the system of **Keaveny et al.** that included the optical input/output connectors of the modules connected by a fiber optic transmission medium such that signals were communicated between the modules in the form of light. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

6.5 As per Claim 5, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 4. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that the module bypass circuit board of the first module outputs electrical signals from the first module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector. **Keaveny et al.** teaches that the module bypass circuit board of the first module outputs electrical signals from the first module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included the module bypass circuit board of the first module outputting electrical signals from the first module to the second module via the optical input/output connector when light signals were received from the second module by the optical input/output connector. The artisan

would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

6.6 As per Claim 7, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem** teaches that the storage devices are disk drives and the storage device bypass circuit boards are disk drive bypass circuit boards each having a connector to receive a disk drive (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Per claim 10: **Leshem** teaches that the controller operates with a Fiber Channel protocol and the controller is Fiber Channel controller (CL2, L30-35; CL3, L33-36; CL3, L40-50).

6.7 As per Claim 11, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem** does not expressly teach that the controller is an arbitrated dual channel Fiber Channel controller. **Dekoning et al.** teaches that the controller is an arbitrated dual channel Fiber Channel controller (CL1, L57-64; CL3, L56-64), as the dual channels provide redundant loops to enhance the reliability of the storage system; so if one loop becomes inoperable, the second loop may remain operational and the information can be diverted to the other loop to enable continued communication with all devices on the redundant loop (CL3, L56-64). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that

included the controller being an arbitrated dual channel Fiber Channel controller. The artisan would have been motivated because the dual channels would provide redundant loops to enhance the reliability of the storage system; so if one loop became inoperable, the second loop might remain operational and the information could be diverted to the other loop to enable continued communication with all devices on the redundant loop.

6.8 As per Claim 12, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 4. **Leshem** teaches that each storage device is a disk drive and wherein each storage device bypass circuit board comprises a disk drive bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach the disk drive bypass circuit board including a circuit which completes the connection of the CPU with the other drive bypass circuits and their associated disk drives whether or not the disk drive is present. **Dekoning et al.** teaches the disk drive bypass circuit board including a circuit which completes the connection of the CPU with the other drive bypass circuits and their associated disk drives whether or not the disk drive is present (Fig 6; CL11, L30-60), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included the disk drive bypass circuit board including a circuit which completes the connection of the CPU with the other drive bypass circuits and their associated disk drives whether or not the disk drive is present. The artisan would have been motivated because that would enable

detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

6.9 As per Claims 13-15, these are system claims having the same limitations as Claims 3-5. Therefore, Claims 13-15 are rejected based on the same reasoning as Claims 3-5, supra.

7. Claims 6, 16, 19-24 and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Keaveny et al.** (U.S. Patent 6,065,087), **Swanson et al.** (U.S. Patent 6,580,531), **Dekoning et al.** (U.S. Patent 6,055,228) and **Harvey** (U.S. Patent 5,831,525).

7.1 As per Claim 6, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 1. **Leshem** teaches the at least one module includes a storage device bypass board connector for each of the storage device bypass circuit boards (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that the at least one module includes a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes. **Harvey** teaches that the at least one module includes a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes

(CL5, L14-50; Fig 1; Fig 2), as that will prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the at least one module includes a storage device bypass board connector for each of the storage device bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and storage devices for cooling purposes. The artisan would have been motivated because that would prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

7.2 As per Claim 16, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 11. **Leshem** teaches that the storage devices are disk drives and the storage device bypass circuit boards are disk drive bypass circuit boards each having a connector to receive a disk drive; and the at least one module includes a disk drive bypass board connector for each of the disk drive bypass circuit boards (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that the at least one module includes a disk drive bypass board connector for each of the disk drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. **Harvey** teaches that the at least one module includes a disk drive bypass board connector for each of the disk drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and

alongside the bypass circuit boards and disk drives for cooling purposes (CL5, L14-50; Fig 1; Fig 2), as that will prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the at least one module including a disk drive bypass board connector for each of the disk drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. The artisan would have been motivated because that would prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

7.3 As per Claim 19, **Leshem** teaches a high speed mass storage system (CL1, L4-8; CL1, L33-37; Abstract, L11-14); comprising at least one module containing:

at least one CPU (Fig 1, Item 22; CL3, L26-27);

a plurality of plug-in storage devices for storing information (Abstract, L1-3; Abstract, L11-17; Fig 1; Fig 2); and

a disk drive bypass circuit board associated with each disk drive (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that high speed mass storage system is adapted to be readily expandable to increase its storage capacity while the system is in operation. **Espy** teaches that high speed mass storage system is adapted to be readily expandable to increase its storage capacity while the system is in operation (Page 1, L19-24), as that will enable to add an

additional disk array chassis to the existing system when additional memory space is required, without shutting down the existing system (Page 1, L19-24). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included high speed mass storage system adapted to be readily expandable to increase its storage capacity while the system was in operation. The artisan would have been motivated because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system.

Leshem does not expressly teach a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into the disk drive connector on the disk drive bypass circuit board. **Harvey** teaches a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into the disk drive connector on the disk drive bypass circuit board (CL5, L14-50; Fig 2, Items 226, 228 and 230), as that will connect the computer's electronic circuitry necessary for operating the data storage device to the circuit board through the multipin connector and through the connector at the other end to the data storage device (CL5, L14-28). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included a disk drive bypass circuit board associated with each disk drive and including a disk drive connector at one edge thereof and a bypass board connector at another edge thereof, each disk drive being plugged into the disk drive connector on the disk drive bypass circuit

board. The artisan would have been motivated because that would connect the computer's electronic circuitry necessary for operating the data storage device to the circuit board through the multipin connector and through the connector at the other end to the data storage device.

Leshem teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach a module bypass circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. **Keaveny et al.** teaches a circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included a circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals. The artisan would have been motivated because that would provide a way to combine the economic

advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

Leshem teaches a controller providing a communication path between the CPU with some of the storage devices through its associated storage device bypass circuit board (CL3, L33-36; CL3, L40-50). **Leshem** does not expressly teach a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board. **Dekoning et al.** teaches a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board (Fig 7; CL3, L36-41), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board. The artisan would have been motivated because that would enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

Leshem does not expressly teach a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the controller with each disk drive bypass circuit board and the module bypass circuit board in the loop. **Espy** teaches a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the controller with each disk drive bypass circuit board and the module

bypass circuit board in the loop (Page 2, L5-23; Fig 1, Item 40; Page 6, L7-16), as that will enable to add an additional disk array chassis to the existing system when additional memory space is required, without shutting down the existing system (Page 1, L19-24). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included a controller connecting the CPU with each of the disk drives through its associated drive bypass circuit board and through the module bypass circuit board such that a loop is formed between the output and input of the controller with each disk drive bypass circuit board and the module bypass circuit board in the loop. The artisan would have been motivated because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system.

Leshem does not expressly teach completing the loop whether or not a disk drive is plugged into the disk drive connector. **Dekoning et al.** teaches completing the loop whether or not a disk drive is plugged into the disk drive connector (Fig 6; CL11, L30-60), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included completing the loop whether or not a disk drive is plugged into the disk drive connector. The artisan would have been motivated because that would enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

7.4 As per Claim 20, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 19. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that a second module connected to the at least one module via the optical input/output connector, the module bypass circuit board of the at least one module completing the loop through the second module. **Keaveny et al.** teaches that a second module connected to the at least one module via the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included a second module connected to the at least one module via the optical input/output connector. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

Espy teaches the module bypass circuit board of the at least one module completing the loop through the second module (Page 2, L5-23; Fig 1, Item 40; Page 6, L7-16), as that will enable to add an additional disk array chassis to the existing system when additional memory space is required, without shutting down the existing system (Page 1, L19-24). It would have

been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included the module bypass circuit board of the at least one module completing the loop through the second module. . The artisan would have been motivated because that would enable to add an additional disk array chassis to the existing system when additional memory space was required, without shutting down the existing system.

7.5 As per Claim 21, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 19. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that the module bypass circuit board outputs electrical signals from the at least one module via the optical input/output connector when light signals are received by the optical input/output connector. **Keaveny et al.** teaches a circuit board that outputs electrical signals from the at least one module via the optical input/output connector when light signals are received by the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem**

including module bypass circuit with the system of **Keaveny et al.** that outputted electrical signals from the at least one module via the optical input/output connector when light signals were received by the optical input/output connector. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

7.6 As per Claim 22, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 20. **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach each of the modules including elements (a) through (e) as discussed in Paragraph 8.3 above. **Leshem** does not expressly teach that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light. **Keaveny et al.** teaches that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** with the system of **Keaveny et al.** that included the optical input/output connectors of the modules connected by a fiber optic transmission medium such that signals were communicated between the modules in the form of

light. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

7.7 As per Claim 23, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 22. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that the module bypass circuit board of the at least one module outputs electrical signals from the at least one module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector. **Keaveny et al.** teaches that the module bypass circuit board of the at least one module outputs electrical signals from the at least one module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at

the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included the module bypass circuit board of the at least one module outputting electrical signals from the at least one module to the second module via the optical input/output connector when light signals were received from the second module by the optical input/output connector. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

7.8 As per Claim 24, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 19. **Leshem** teaches that the at least one module includes a drive bypass board connector for each of the drive bypass circuit boards (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that the at least one module includes a drive bypass board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. **Harvey** teaches that the at least one module includes a drive bypass board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes (CL5, L14-50; Fig 1; Fig 2), as that will prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the

time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the at least one module including a drive bypass board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors and alongside the bypass circuit boards and disk drives for cooling purposes. The artisan would have been motivated because that would prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

Per claim 28: **Leshem** teaches that the controller operates with a Fiber Channel protocol and the controller is Fiber Channel controller (CL2, L30-35; CL3, L33-36; CL3, L40-50).

7.9 As per Claim 29, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 19. **Leshem** does not expressly teach that the controller is an arbitrated dual channel Fiber Channel controller. **Dekoning et al.** teaches that the controller is an arbitrated dual channel Fiber Channel controller (CL1, L57-64; CL3, L56-64), as the dual channels provide redundant loops to enhance the reliability of the storage system; so if one loop becomes inoperable, the second loop may remain operational and the information can be diverted to the other loop to enable continued communication with all devices on the redundant loop (CL3, L56-64). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included the controller being an arbitrated dual channel Fiber Channel controller. The artisan would have been motivated because the dual channels would provide redundant loops to enhance the reliability of the storage system; so if one loop became inoperable, the second loop might

remain operational and the information could be diverted to the other loop to enable continued communication with all devices on the redundant loop.

7.10 As per Claim 30, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 29. **Leshem** does not expressly teach that each drive bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present. **Dekoning et al.** teaches that each drive bypass circuit board includes a circuit which completes the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device is present (Fig 6; CL11, L30-60), as that will enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device (CL11, L40-60). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Dekoning et al.** that included each drive bypass circuit board including a circuit which completed the connection of the CPU with the other storage device bypass circuits and their associated storage devices whether or not the storage device was present. The artisan would have been motivated because that would enable detection of failure or absence of a storage device and bypassing the storage device by connecting the daisy chain loop without the device.

7.11 As per Claim 31, it is a system claim having the same limitations as Claim 21. Therefore, Claim 31 is rejected based on the same reasoning as Claim 21, supra.

7.12 As per Claim 32, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 29. **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach first and second modules each including elements (a) through (e) as discussed in Paragraph 8.3 above. **Leshem** does not expressly teach that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light. **Keaveny et al.** teaches that the optical input/output connectors of the modules are connected by a fiber optic transmission medium such that signals are communicated between the modules in the form of light (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** with the system of **Keaveny et al.** that included the optical input/output connectors of the modules connected by a fiber optic transmission medium such that signals were communicated between the modules in the form of light. The artisan would have been motivated because that would provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

7.13 As per Claim 33, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 32. **Leshem** teaches a module bypass circuit board (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A) and fiber communication channel between the disk controllers and the disk interfaces (Fig 2A; CL3, L33- 50). **Leshem** does not expressly teach that the module bypass circuit board of the first module outputs electrical signals from the first module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector. **Keaveny et al.** teaches that the module bypass circuit board of the first module outputs electrical signals from the first module to the second module via the optical input/output connector when light signals are received from the second module by the optical input/output connector (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the system of **Leshem** including module bypass circuit with the system of **Keaveny et al.** that included the module bypass circuit board of the first module outputting electrical signals from the first module to the second module via the optical input/output connector when light signals were received from the second module by the optical input/output connector. The artisan would have been motivated because that would provide a way to combine the economic

advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel.

7.14 As per Claim 34, it is a system claim having the same limitations as Claim 24. Therefore, Claim 34 is rejected based on the same reasoning as Claim 24, supra.

8. Claims 8, 9, 17, 18, 25-27, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leshem** (U.S. Patent 5,729,763) in view of **Espy** (International Application WO 98/21660), and further in view of **Keaveny et al.** (U.S. Patent 6,065,087), **Swanson et al.** (U.S. Patent 6,580,531), **Dekoning et al.** (U.S. Patent 6,055,228), **Harvey** (U.S. Patent 5,831,525) and **Kimura et al.** (U.S. Patent 5,414,591).

8.1 As per Claim 8, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al.** teach the system of claim 7. **Leshem** teaches the at least one module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that the at least one module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors. **Harvey** teaches that the at least one module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors (CL5, L14-50; Fig 1; Fig 2), as that will prevent overheating of the drive and the

drive related computer hardware and loss of valuable data (CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the at least one module including a disk drive bypass circuit board connector for each of the drive bypass circuit boards with an opening between each connector to permit the flow of air between the connectors. The artisan would have been motivated because that would prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

Leshem does not expressly teach that each drive bypass circuit board is a relatively flat circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector. **Harvey** teaches that each drive bypass circuit board is a circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector (CL5, L14-50; Fig 2, Items 226, 228 and 230), as that will connect the computer's electronic circuitry necessary for operating the data storage device to the circuit board through the multipin connector and through the connector at the other end to the data storage device (CL5, L14-28). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included each drive bypass circuit board being a circuit board with a connector on opposite edges, wherein one of the connectors was the connector which received the disk drive and the other connector connected to the drive bypass circuit board connector. The artisan would have been motivated because that would connect the computer's electronic circuitry necessary for operating the data storage device

to the circuit board through the multipin connector and through the connector at the other end to the data storage device.

Leshem does not expressly teach that each drive bypass circuit board is a relatively flat circuit board. **Kimura et al.** teaches that each drive bypass circuit board is a relatively flat circuit board (Fig 19; Fig 20; CL11, L19-52), as that will allow the cooling air that has cooled the disk drive to flow over the circuit board, the board being along the cooling air flow (CL11, L34-38). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Kimura et al.** that included each drive bypass circuit board being a relatively flat circuit board. The artisan would have been motivated because that would allow the cooling air that has cooled the disk drive to flow over the circuit board, the board being along the cooling air flow.

Leshem does not expressly teach the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. **Harvey** teaches the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction (CL5, L14-20; Fig 1; Fig 2), as that will improve the hard drive and circuit board cooling and prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL1, L60-62; CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the connectors, bypass circuit boards

and drives being arranged such that when they were connected there was a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. The artisan would have been motivated because that would improve the hard drive and circuit board cooling and prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

8.2 As per Claim 9, **Leshem, Espy, Keaveny et al., Swanson et al.** and **Dekoning et al., Harvey** and **Kimura et al.** teach the system of claim 8. **Leshem** does not expressly teach that the module is housed in an enclosure and at least one fan is mounted to force air from outside the enclosure through the spaces between the bypass boards and drives. **Espy** teaches that the module is housed in an enclosure and at least one fan is mounted to force air from outside the enclosure through the spaces between the bypass boards and drives (Page 5, L16-19), as the disk array chassis provides a series of openings into which several disk drives may be inserted (Page 5, L15-17); and as per **Harvey**, the fan provides air flow through the drive module and around the circuit board (CL5, L35-50). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Espy** that included the module being housed in an enclosure and at least one fan being mounted to force air from outside the enclosure through the spaces between the bypass boards and drives. The artisan would have been motivated because the disk array chassis would provide a series of openings into which several disk drives could be inserted and the fan would provide air flow through the drive module and around the circuit board.

8.3 As per Claims 17-18, these are system claims having the same limitations as Claims 8-9. Therefore, Claims 17-18 are rejected based on the same reasoning as Claims 8-9, supra.

8.4 As per Claim 25, **Leshem, Espy, Keaveny et al., Swanson et al., Dekoning et al.** and **Harvey** teach the system of claim 19. **Leshem** teaches the at least one module includes a disk drive bypass circuit board connector for each of the drive bypass circuit boards (CL1, L65 to CL2, L3; CL2, L36-41; CL2, L53-60; CL4, L26-67; Fig 2A).

Leshem does not expressly teach that each drive bypass circuit board is a relatively flat circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector. **Harvey** teaches that each drive bypass circuit board is a circuit board with a connector on opposite edges, wherein one of the connectors is the connector which receives the disk drive and the other connector connects to the drive bypass circuit board connector (CL5, L14-50; Fig 2, Items 226, 228 and 230), as that will connect the computer's electronic circuitry necessary for operating the data storage device to the circuit board through the multipin connector and through the connector at the other end to the data storage device (CL5, L14-28). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included each drive bypass circuit board being a circuit board with a connector on opposite edges, wherein one of the connectors was the connector which received the disk drive and the other connector connected to the drive bypass circuit board connector. The artisan would have been motivated because that would connect the computer's electronic circuitry necessary for operating the data storage device

to the circuit board through the multipin connector and through the connector at the other end to the data storage device.

Leshem does not expressly teach that each drive bypass circuit board is a relatively flat circuit board. **Kimura et al.** teaches that each drive bypass circuit board is a relatively flat circuit board (Fig 19; Fig 20; CL11, L19-52), as that will allow the cooling air that has cooled the disk drive to flow over the circuit board, the board being along the cooling air flow (CL11, L34-38). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Kimura et al.** that included each drive bypass circuit board being a relatively flat circuit board. The artisan would have been motivated because that would allow the cooling air that has cooled the disk drive to flow over the circuit board, the board being along the cooling air flow.

Leshem does not expressly teach the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. **Harvey** teaches the connectors, bypass circuit boards and drives being arranged such that when they are connected there is a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction (CL5, L14-20; Fig 1; Fig 2), as that will improve the hard drive and circuit board cooling and prevent overheating of the drive and the drive related computer hardware and loss of valuable data (CL1, L60-62; CL2, L1-6). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Leshem** with the system of **Harvey** that included the connectors, bypass circuit boards

and drives being arranged such that when they were connected there was a path for air flow from outside the module alongside each bypass circuit board and its associated disk drive for cooling purposes without any backplane obstruction. The artisan would have been motivated because that would improve the hard drive and circuit board cooling and prevent overheating of the drive and the drive related computer hardware and loss of valuable data.

8.5 As per Claim 26, it is a system claim having the same limitations as Claim 9. Therefore, Claim 26 is rejected based on the same reasoning as Claim 9, supra.

8.6 As per Claim 27, **Leshem** teaches that each drive bypass circuit board connector is mounted in the same plane in spaced relationship with each other (Fig 2A).

8.7 As per Claims 35-36, these are system claims having the same limitations as Claims 25-26. Therefore, Claims 35-36 are rejected based on the same reasoning as Claims 25-26, supra.

Response to Arguments

9. As per the applicants' argument that "there is no teaching , disclosure or suggestion in Epsey of an optical input/output connector for outputting electrical signals as light signals and for inputting light signals as electrical signals; Deckoning et al. does not teach, disclose or suggest that the shunt includes an optical input/output connector for outputting electrical signals as light signals and for inputting light signals as electrical signals; Harvey does not teach,

disclose or suggest that the shunt includes an optical input/output connector for outputting electrical signals as light signals and for inputting light signals as electrical signals; and Kimura et al. does not teach, disclose or suggest that the shunt includes an optical input/output connector for outputting electrical signals as light signals and for inputting light signals as electrical signals;", the Examiner has used new references **Keaveny et al.** and **Swanson et al.**

Keaveny et al. teaches a circuit board including an optical input/ output connector for outputting electrical signals from the module as light signals and for inputting light signals into the module as electrical signals (Fig 9, Item 902 and 908; CL13, L18-36), as that will provide a way to combine the economic advantages of the SCSI compatible mass storage devices with the high connectivity and high bandwidth and greatly increased physical distance of accessibility provided by the fiber channel (CL13, L35-40); and as per **Swanson et al.** the optical connector is an optical transceiver which receives as input an electrical signal in the form of high speed serial bit stream and outputs a modulated light signal and transforms the received light signal into an electrical serial bit stream (CL1, L18-42).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043, till October 27, 2004 and 571-272-3717 after October 27, 2004. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704, till October 27, 2004 and 571-272-3716 after October 27, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
October 19, 2004